PS310DV Digital Proximity Sensor with VCSEL

1. Features

- Proximity Detection
  - Programmable Offset Control Register
  - Programmable Analog Gain and Integration Time
  - Integrated LED Driver and VCSEL
- Power Management
  - Low Power 1uA Sleep State
  - 70uA Wait State with Programmable Wait Time from 3ms to 10seconds
- I2C Interface Compatible
  - Up to 400kHz (I2C Fast Mode)
  - Device addr. : 0x39 (7bit)

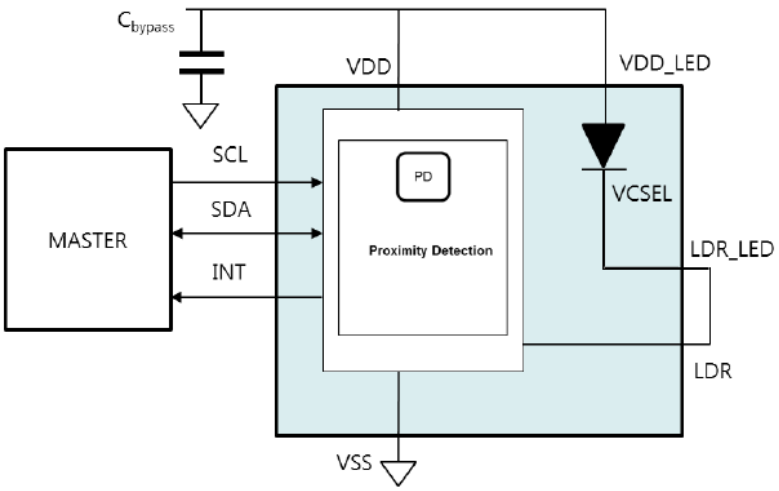
2. Applications

- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement
- Automatic Speakerphone Enable
- Automatic Menu Popup

3. Description

The proximity detection feature allows a large dynamic range of operation for use in short distance detection behind dark glass such as in a cell phone or for longer distance measurements for applications such as presence detection for monitors or laptops. The programmable proximity detection enables continuous measurements across the entire range. In addition, an internal state machine provides the ability to put the device into a low power mode measurements providing very low average power consumption.

Simplified Schematic



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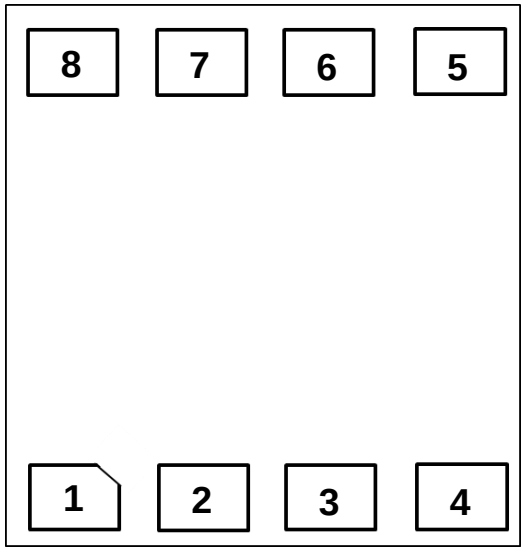


TOP View

Pin Functions

#	PIN	I/O/P/G	DESCRIPTION
1	SDA	I/O	I2C serial data input/output terminal
2	SCL	I	I2C serial clock input terminal
3	LDR	O	Proximity VCSEL controlled current sink driver
4	VSS	G	Supply Ground
5	INT	O	Interrupt – open drain (active low)
6	VDD	P	Supply voltage
7	VDD_LED	P	Supply voltage for VCSEL
8	LDR_LED	O	Proximity VCSEL controlled current sink driver

5. Specifications

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Power Supply Voltage	-0.3	6	V
Vin	Input Voltage	-0.3	VDD	V
Vout	Output Voltage	-0.3	VDD	V
Vhbm	Static Discharge (HBM)		2000	V
Vmm	Static Discharge (MM)		200	V
Tj	Junction Temperature	-40	125	℃

+ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 1: All voltage values are with respect to VSS.

5.2 Recommended Operating Conditions

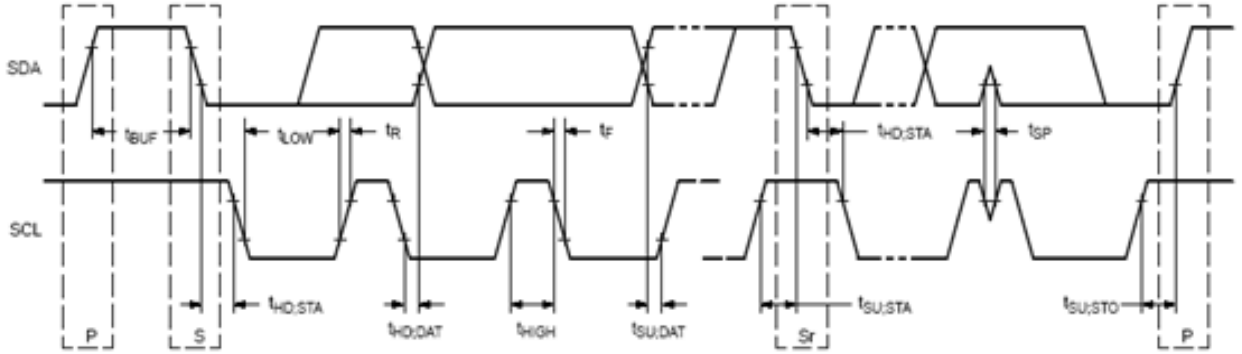
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD	Power Supply Voltage	2.7	3.0	5	V
Vin	Input Voltage	0		VDD	V
Vout	Output Voltage	0		VDD	V
TA	Operating ambient temperature	-40		85	℃

5.3 Electrical Characteristics (VDD = 3V, Ta = 25℃)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	Active – LDR pulses off		158		uA
	Wait state		55		
	Sleep state		1	10	
INT, SDA output low voltage	3mA sink current 6mA sink current	0 0		0.4 0.6	V
Low Level Input Voltage				0.3VDD	V
High Level Input Voltage		0.7VDD			V

5.4 Data Transmission Timing Requirements

PARAMETER	Symbol	CONDITIONS	MIN	MAX	UNIT
Output Low Level (SDA)	V_{OL}	IOL = 4mA		0.5	V
SCLK Operating Frequency	f_{SCLK}			400	kHz
Stop and Start Condition	t_{BUF}		1.3		us
Hold Time After Repeated Start Conditions	$t_{HD;STA}$		0.6		us
SCLK Clock Low Period	t_{LOW}		1.3		us
SCLK Clock High Period	t_{HIGH}		0.6		us
Repeated Start Condition Setup Time	$t_{SU;STA}$		0.6		us
Data Hold Time	$t_{HD;DAT}$		0	0.9	us
Data Setup Time	$t_{SU;DAT}$		100		ns
Clock/Data Fall Time	t_F			300	ns
Clock/Data Rise Time	t_R			300	ns
Stop Condition Setup Time	$t_{SU;STO}$		0.6		us



5.5 Proximity Characteristics (VDD = 3V, Ta = 25℃, PEN = 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Prox. Full count value					65535	counts
LED drive current	PDH = 0	PDRIVE = 0 PDRIVE = 1 PDRIVE = 2 PDRIVE = 3		125 100 75 50		mA
	PDH = 1	PDRIVE = 0 PDRIVE = 1 PDRIVE = 2 PDRIVE = 3		12.5 10 7.5 5		mA
Prox. offset	PDRIVE = 0				4	counts

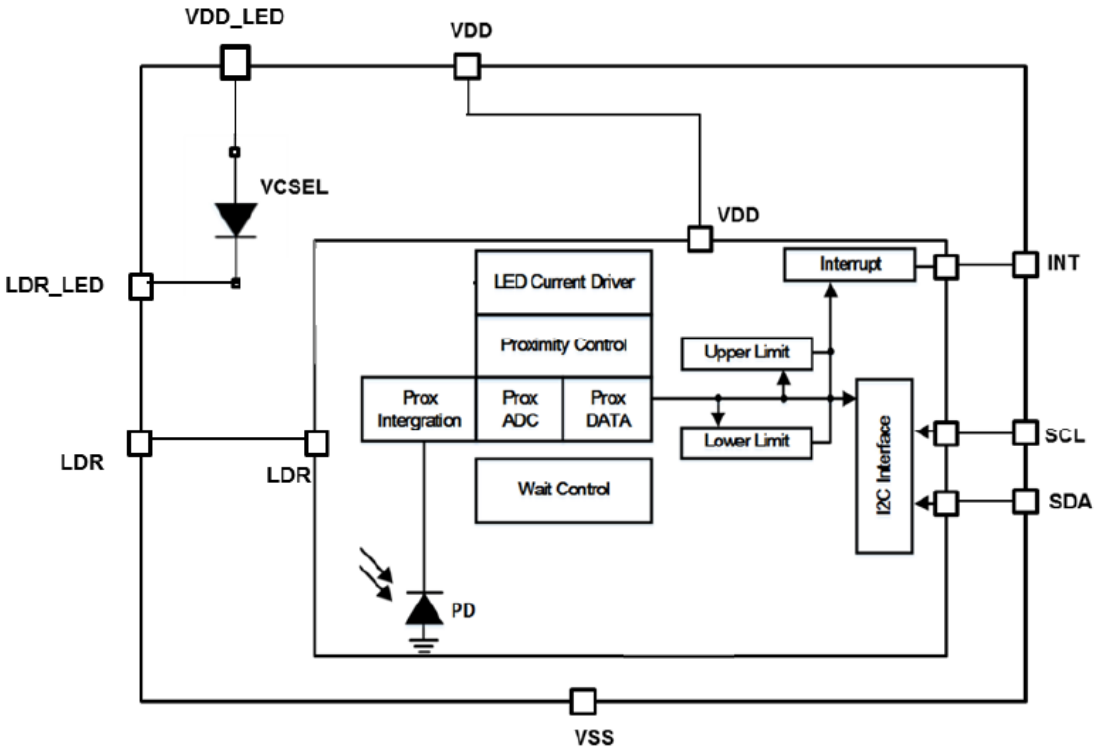
6. Detailed Description

6.1 Overview

The PS310DV provides on-chip photo diode, integrating amplifier, ADC, accumulator, clock, buffer, comparator, a state machine and an I2C interface. Also It has VCSEL integrated. Integrating ADC simultaneously convert the amplified photodiode currents into a digital value providing up to 16 bits of resolution.

The device is standby I2C interface which supports up to 400-kbits/s data rate. The digital interface supports IO levels from 2.7V to 5.0V.

6.2 Function Block Diagram



6.3 Feature Description

6.3.1 System State machine

An internal state machine provides system control of the proximity detection, power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I2C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity function is enabled. Once enabled, the device will execute the Prox., Wait states in sequence as indicated in Figure 1. Upon completion and return to Idle, the device will automatically begin a new prox.-wait cycle as long as PON and either PEN remain enabled.

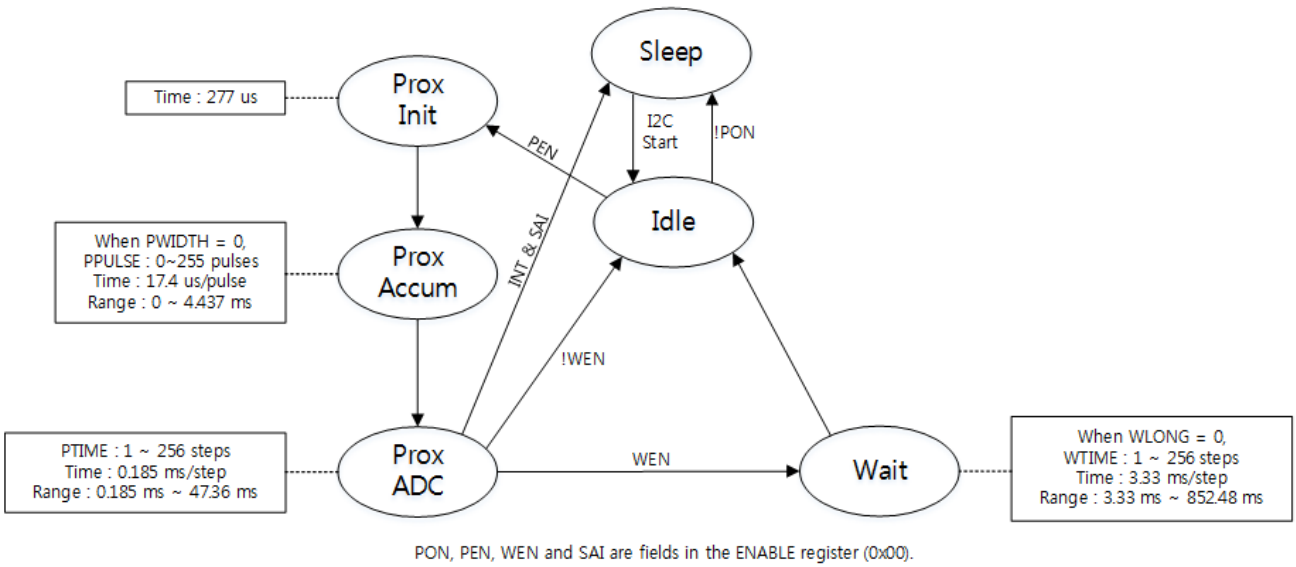


Figure 1. State Diagram

6.3.2 Proximity Detection

Proximity detection is accomplished by measuring the amount of light energy, generally from an VCSEL, reflected off an object to determine its distance. The proximity light source, which is external to the PS310DV device, is driven by the integrated proximity LED current driver as shown in Figure 2.

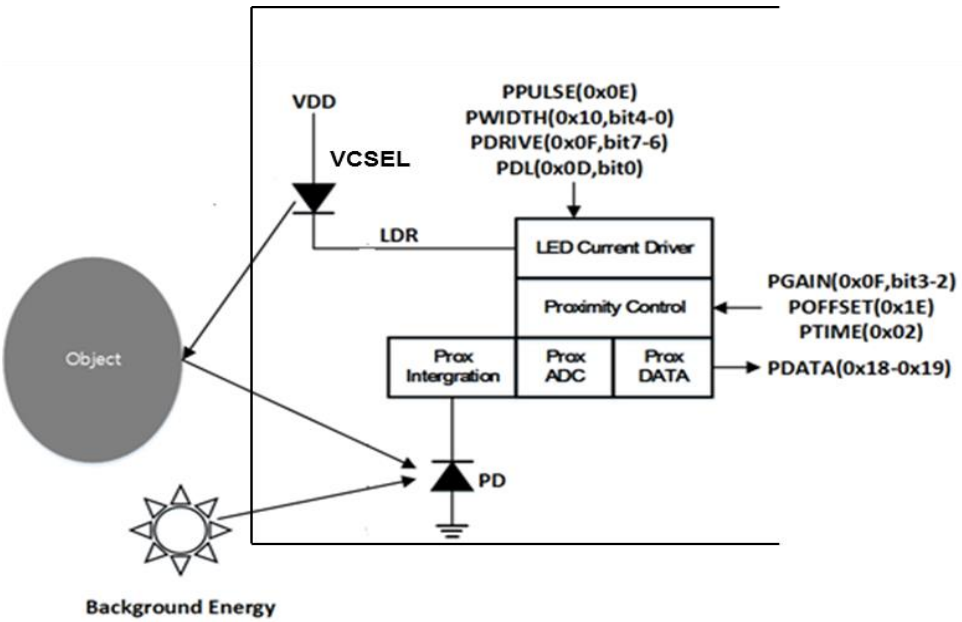


Figure 2. Proximity Detection

The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. The combination of proximity LED drive strength (PDRIVE) determine the drive current. PDRIVE sets the drive current to 125mA, 100mA, 75mA, or 50mA. To drive an external light source with more than 125 mA or to minimize on-chip ground bounce, LDR can be used to drive an external p-type transistor, which in turn drives the light source.

6.3.3 Interrupt

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for proximity values outside a user-defined range. While the interrupt function is always enabled and its status is available in the Status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) field in the Enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired proximity range. An interrupt can be generated when the proximity data (PDATA) is less than the proximity interrupt low threshold (PILTx) or is greater than the proximity interrupt high threshold (PIHTx).

To further control when an interrupt occurs, the device provides an interrupt persistence feature. The persistence filter allows the user to specify the number of consecutive out-of-range proximity occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values.

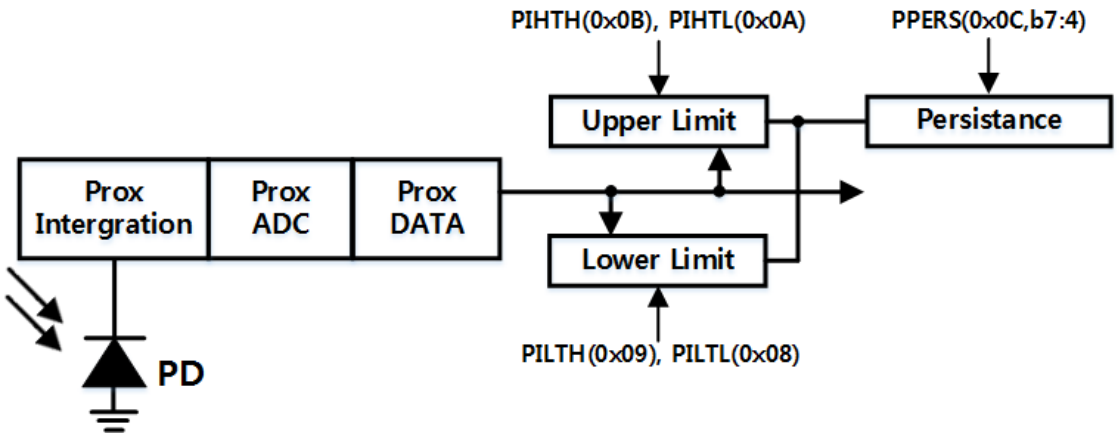


Figure 3. Programmable Interrupt

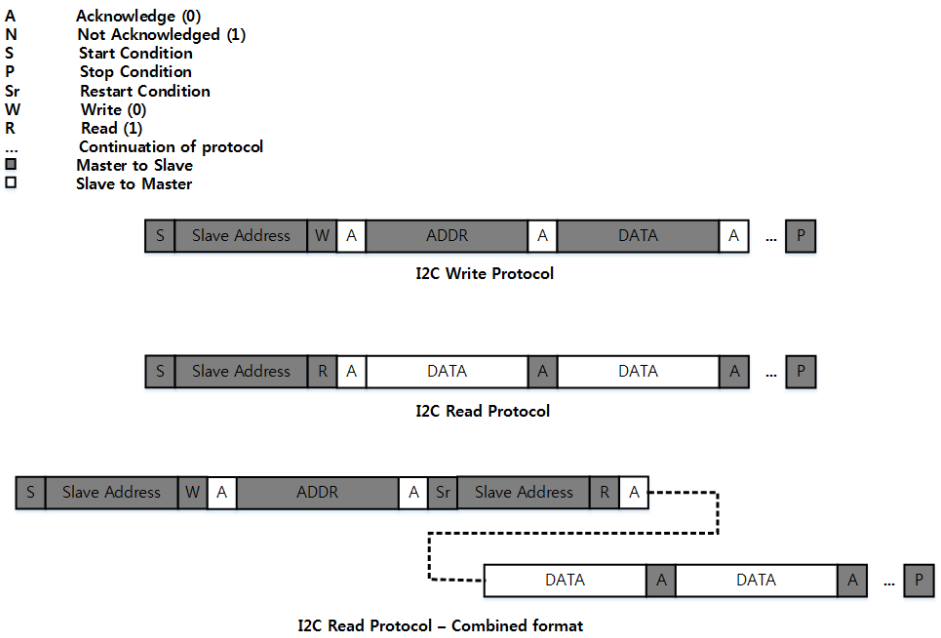
6.4 Programming

6.4.1 I2C Protocol

Interface and control of the PD310DH is accomplished through an I2C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x39 hex using 7-bit addressing protocol. (Contact factory for other addressing options.)

The I2C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 4). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

For a complete description of I2C protocols, please review the I2C Specification at: http://www.semiconductors.philips.com.



< Figure 4. I2C Protocols>

6.5 Register Maps

ADDRESS	NAME	R/W	REGISTER FUNCTION	DEFAULT
-	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	RW	Enable states and interrupts	0x00
0x02	PTIME	RW	Proximity time	0xFF
0x03	WTIME	RW	Wait time	0xFF
0x08	PILTL	RW	interrupt low threshold low byte	0x00
0x09	PILTH	RW	interrupt low threshold high byte	0x00
0x0A	PIHTL	RW	interrupt high threshold low byte	0x00
0x0B	PIHTH	RW	interrupt high threshold high byte	0x00
0x0C	PERS	RW	Interrupt persistence filter	0x00
0x0D	CONFIG	RW	Configuration	0x00
0x0E	PPCOUNT	RW	Pulse count	0x00
0x0F	CONTROL	RW	Control register	0x00
0x10	PWIDTH	RW	Pulse width	0x00
0x12	ID	R	Device ID	0x03
0x13	STATUS	R	Device status	0x00
0x18	PDATAL	R	Proximity data low byte	0x00
0x19	PDATAH	R	Proximity data high byte	0x00
0x1E	POFFSET	RW	Proximity Offset register	0x00
0xE5	INTCLEAR	W	Interrupt clear	0x00

6.5.1 ADDR(COMMAND) Register

The ADDR (COMMAND) register specifies the address of the target register for future read and write operations, as well as issues special function commands.

	7	6	5	4	3	2	1	0	
ADDR	**SEL**	**TYPE**		**ADDR/SF**					**Default 0x00**

FIELD	BITS	DESCRIPTION (Default = 0x00)	
SEL	7	Select SF/ADDR Register.	
		FIELD VALUE	**DESCRIPTION**
		0	Address Select
		1	Special Function Select
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**DESCRIPTION**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
ADDR /SF	4:0	Address field/special function field. The field values listed below apply only to special function commands:	
		FIELD VALUE	**DESCRIPTION**
		00101	interrupt clear
		other	Reserved — Do not use

6.5.2 ENABLE Register (0x00)

The enable register is used to power the device on/off, enable functions, and interrupts.

	7	6	5	4	3	2	1	0	
ENABLE	Reserved	SAI	PIEN	Reserved	WEN	PEN	Reserved	PON	Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of a proximity cycle if an interrupt has been generated.
PIEN	5	Proximity interrupt Enable. When asserted permits proximity interrupts to be generated, subject to the persist filter.
Reserved	4	Reserved. Write as 0.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
Reserved	1	Reserved. Write as 0.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channel to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

6.5.3 PTIME Register (0x02)

The proximity time register controls the integration time of the proximity ADC in 0.185 ms increments. Upon power up, the proximity time register is set to 0xFF. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

FIELD	BITS	DESCRIPTION (Default = 0xFF)		
PTIME	7:0	VALUE	INTEG_CYCLES	TIME
		0xFF	1	0.185 ms
		0xFE	2	0.390 ms
		...	...	...
		0x00	256	47.36 ms

6.5.4 WTIME Register (0x03)

Wait time is set 3.33 ms increments unless the WLONG bit is asserted in which case the wait times are 12 × longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

FIELD	BITS	DESCRIPTION (Default = 0xFF)			
		VALUE	WAIT TIME	TIME(WLONG=0)	TIME(WLONG=1)
WTIME	7:0	0xFF	1	3.33 ms	0.04 sec
		0xFE	2	6.66 ms	0.08 sec
		…	…	…	…
		0x00	256	852.48 ms	10.2 sec

6.5.5 Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the upper and lower threshold values to the proximity interrupt comparators. See Interrupts in the Principles of Operation section for detailed information. Upon power up, the interrupt threshold registers reset to 0x00.

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity interrupt low threshold low byte
PILTH	0x09	7:0	Proximity interrupt low threshold high byte
PIHTL	0x0A	7:0	Proximity interrupt high threshold low byte
PIHTH	0x0B	7:0	Proximity interrupt high threshold high byte

6.5.6 Interrupt Persistence Filter Register (0x0C)

The interrupt persistence filter sets the number of consecutive proximity cycles that are out-of-range before an interrupt is generated. Out-of-range is determined by the proximity interrupt threshold registers (0x08 through 0x0B). See Interrupts in the Principles of Operation section for further information. Upon power up, the interrupt persistence filter register resets to 0x00, which will generate an interrupt at the end of each proximity cycle.

	7	6	5	4	3	2	1	0	
PERS	PPERS				Reserved				Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)	
PPERS	7:4	Proximity persistence. Controls rate of proximity interrupt to the host processor.	
		FIELD VALUE	INTERRUPT PERSISTENCE FUNCTION
		0000	Every proximity cycle generates an interrupt
		0001	1 proximity value out of range
		0010	2 consecutive proximity values out of range
		…	…
		1111	15 consecutive proximity values out of range
Reserved	3:0	Reserved. Write as 0.	

6.5.7 Configuration Register (0x0D)

The configuration register sets the proximity LED drive level and wait long time.

	7	6	5	4	3	2	1	0	
CONFIG	Reserved						WLONG	PDH	Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12 × from that programmed in the WTIME register.
PDH	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 10

6.5.8 Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state.

FIELD	BITS	DESCRIPTION (Default = 0x00)
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

6.5.9 Control Register (0x0F)

The configuration register sets the proximity LED drive level and wait long time.

	7	6	5	4	3	2	1	0	
CONTROL	PDRIVE		Reserved		PGAIN		Reserved		Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)		
PDRIVE	7:6	Proximity LED Drive Strength.		
		FIELD VALUE	PDH = 0	PDH = 1
		00	125mA	12.5mA
		01	100mA	10mA
		10	75mA	7.5mA
		11	50mA	5.0mA
Reserved	5:4	Reserved. Write as 0.		
PGAIN	3:2	Proximity Gain.		
		FIELD VALUE	PROXIMITY GAIN VAULE	
		00	1X Gain	
		01	2X Gain	
		10	4X Gain	
		11	8X Gain	
Reserved	1:0	Reserved. Write as 0.		

6.5.10 Pulse Width Register (0x10)

The pulse width register sets the width of proximity pulses that the LDR pin will generate during the Prox Accum state.

	7	6	5	4	3	2	1	0	
PWIDTH	**Reserved**				**PWIDTH**				**Default 0x00**

FIELD	BITS	DESCRIPTION (Default = 0x00)	
Reserved	7:4	Reserved. Write as 0.	
PWIDH	3:0	Proximity Width. 17.4us x (2 ^ PWIDTH)	
		FIELD VALUE	**PROXIMITY PERIOD TIME**
		0000	17.4 us
		0001	34.8 us
		0010	69.6 us
		…	…
		1000	4454.4 us
		Reserved	Reserved

6.5.11 ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

FIELD	BITS	DESCRIPTION (Default = 0x03)
ID	7:0	Part number identification : 0x03 = SO6103

6.5.12 STATUS Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

	7	6	5	4	3	2	1	0	
STATUS	Reserved		PINT	Reserved			PVALID	Reserved	Default 0x00

FIELD	BITS	DESCRIPTION (Default = 0x00)
Reserved	7:6	Reserved. Read as 0.
PINT	1	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
Reserved	4:3	Reserved. Read as 0.
PVALID	1	Proximity Valid. Indicates that the proximity channel has completed an integration cycle after PEN has been asserted
Reserved	0	Reserved. Read as 0.

6.5.13 Proximity Data Registers (0x18 – 0x19)

Proximity data is stored as a 16-bit value. The simplest way to read both bytes is to perform a two-byte I2C read operation using the auto-increment protocol, which is set in the ADDR register TYPE field.

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

6.5.14 Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1).

	7	6	5	4	3	2	1	0	
POFFSET	**SIGN**	**MAGNITUDE**							**Default 0x00**

FIELD	BITS	DESCRIPTION (Default = 0x00)
SIGN	7	Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

6.5.15 Interrupt clear Register (0xE5)

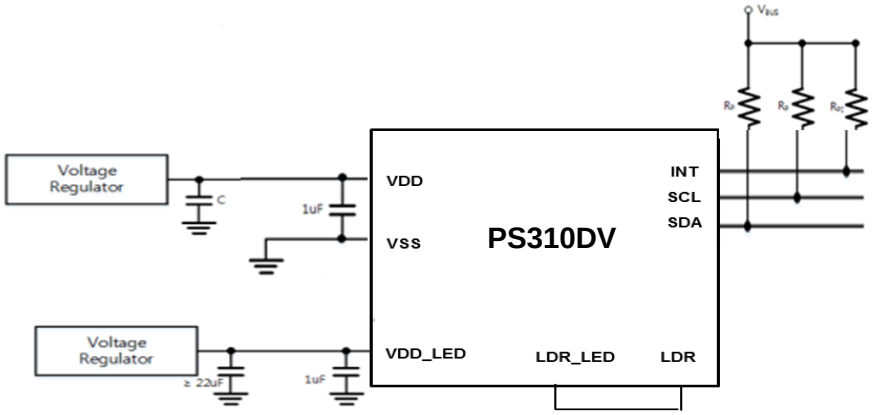
Interrupts are cleared by writing 0x00 to the Interrupt clear Register(0xE5).

Ex) I2C_WriteByte(0x72, 0xE5, 0x00); // interrupt clear

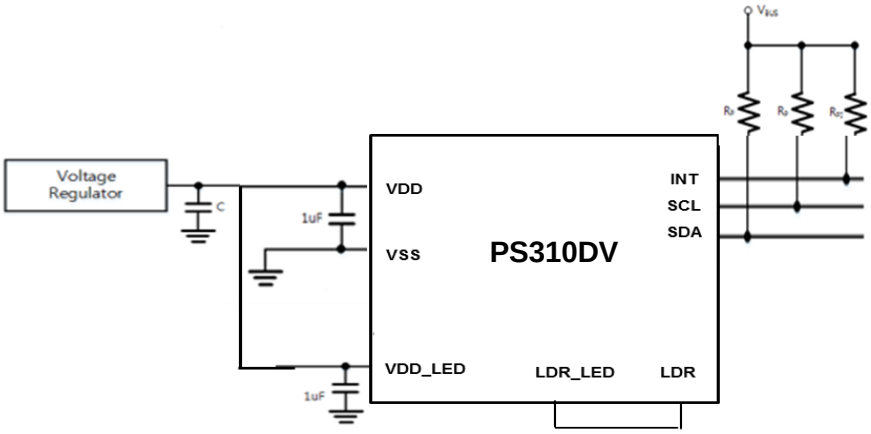
7. Application

7.1 Typical Application

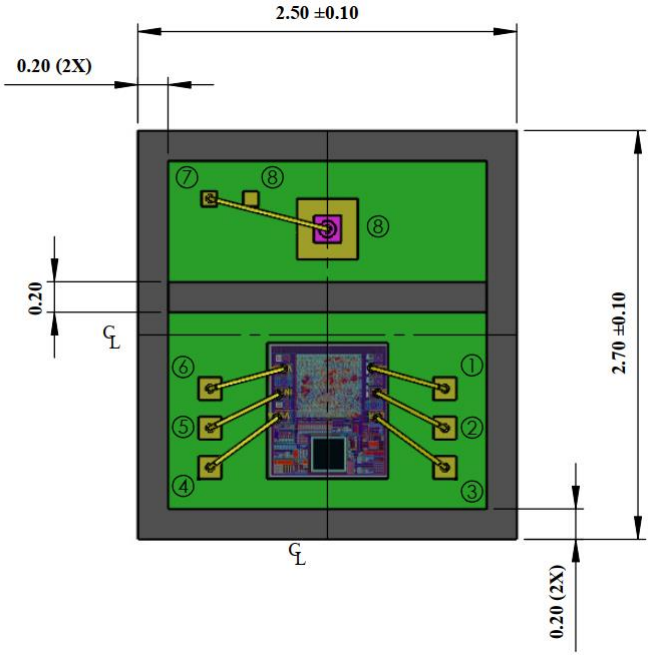
In a proximity sensing system, the VCSEL can be pulsed by the PS310DV with more than 125 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulse.



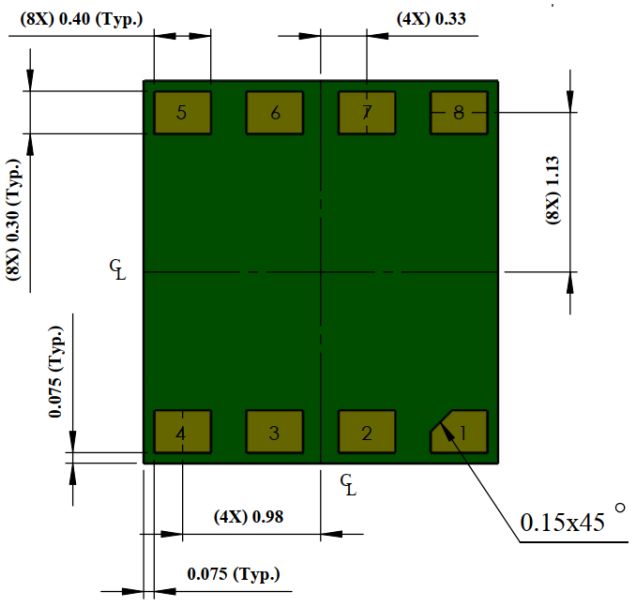
If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22Ω resistor in series with the VDD supply line and a 1-uF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.



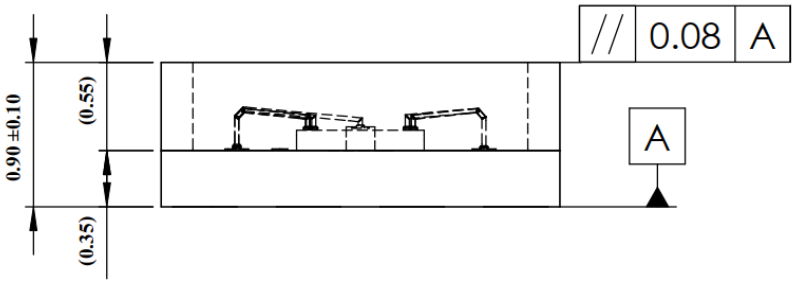
8. Package Dimension



Top view



Bottom view



Side view

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